REMARKS

Claims 1-3 and 6-8, 11 and 12 are pending in the present application. Claims 1-3 and 6-13 were rejected in the Final Office Action mailed June 8, 2006. Claims 9, 10 and 13 are canceled herein without prejudice. Claims 8 and 12 are amended herein. No new matter is introduced as a result of these claim amendments. The Examiner's rejections are traversed below. Applicants respectfully request the Examiner to consider and allow the remaining claims.

Claim Rejections - 35 USC § 103

Claims 1-3 and 6-13

Claims 1-3 and 6-13 were rejected under 35 USC 103(a) as being unpatentable over Mehrad et al. (U.S. Patent No. 6,765,257; hereinafter "Mehrad") in view of Ito et al (U.S. Patent No. 6,700,176; hereinafter "Ito"). Claims 9, 10 and 13 are cancelled herein without prejudice. Claim 8 is amended herein to include the limitations originally recited in claims 9 and 10, and claim 12 is amended herein to include the limitations originally recited in claim 13. Claims 1 and 8 (as amended) require: (a) a region under a stacked gate structure comprising overlapping lateral diffusions of source and drain implantation regions; and (b) a common source line coupled with said source, wherein a source contact disposed

outside of said common source line is coupled with said source, wherein said source contact is coupled to said common source line under said stacked gate structure, and wherein said source contact is disposed in a row with drain contacts.

Mehrad teaches an array of conventional flash memory cells having a common source line coupled with the sources of the cells, and a source contact disposed outside of the common source line and coupled with the source. Ito teaches a MOSFET device 100 having a region under a stacked gate structure comprising overlapping lateral diffusions of source and drain regions. However, there is no motivation to combine Mehrad and Ito.

First, there is no motivation in Mehrad to diffuse the source and drain regions to make a region under the stacked gate of overlapping source and drain regions, as claims 1 and 8 require. In contrast, Mehrad teaches using only "conventional processing" to implant the source and drain areas (col. 3, lines 36-38 and col. 4, lines 13-18). Mehrad fails to teach or suggest the possibility or benefit of overlapping the source and drain regions, as claims 1 and 8 require.

Second, Ito teaches overlapping source and drain regions, but fails to teach or suggest the common source line structure required in claims 1 and 8. Ito teaches only a single MOSFET device 100, and fails to teach or suggest any

arrangement for an array of multiple MOSFET devices 100. There is no motivation in Ito to have a common source line coupled with a source, wherein a source contact disposed outside of the common source line is coupled with the source, wherein the source contact is coupled to the common source line under a stacked gate structure, and wherein the source contact is disposed in a row with drain contacts, as claims 1 and 8 require.

Applicants respectfully assert that the only way for one of ordinary skill in the art to arrive at the present claimed invention as recited in claims 1 and 8 by combining Mehrad and Ito is by using the present application and claims as a blueprint. Thus, Applicants respectfully assert that the rejection of claims 1 and 8 under 35 U.S.C. 103(a) as being unpatentable over Mehrad in view of Ito is traversed, and that claims 1 and 8 are now in condition for allowance. Claims 2, 3, 6 and 7 are dependent on claim 1 and recite additional limitations. Claims 11 and 12 are dependent on claim 8 and recite additional limitation. Therefore, Applicants assert that the rejection of claims 2, 3, 6 , 7, 11 and 12 is also traversed, and that claims 2, 3, 6, 7, 11 and 12 are in condition for allowance.

CONCLUSION

In light of the response presented herein, Applicants respectfully assert that Claims 1-3, 6-8, 11 and 12 of the present application overcome the rejections of record, and therefore earnestly solicit allowance of these claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
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